TDB-ACC-NO: NN8907370

DISCLOSURE TITLE: Breakpoint Bit Technique for an Address Compare Function

PUBLICATION-DATA: IBM Technical Disclosure Bulletin, July 1989, US

VOLUME NUMBER: 32

ISSUE NUMBER: 2

PAGE NUMBER: 370 - 371

PUBLICATION-DATE: July 1, 1989 (19890701)

CROSS REFERENCE: 0018-8689-32-2-370

DISCLOSURE TEXT:

- This article describes a technique which provides a breakpoint function in a processor without the use of extra comparison logic and with minimal delay. - A circuit designed for tracing the address flow of a processor (microprocessor, digital signal processor, etc.) must make an address comparison to begin or stop a trace. To do this a trigger address or breakpoint is usually written to a breakpoint register. This register is periodically compared to the address on the processor's address bus. If a match is detected by a comparator circuit, a breakpoint is found and the address trace logic can begin or halt a trace. This same technique is typically used in stop-on-address circuits to halt a processor at a given address. - The logic required to perform a breakpoint detection typically consists of a breakpoint register and a comparator as shown in Fig. 1. The size of the breakpoint register and comparator depends on the size of the address bus being monitored. For example, on a 14-bit address bus, the register and comparator could easily take up over 100 logic gates if implemented in very large-scale integration (VLSI). - The faster the processor, the faster the comparison must be made. This is extremely important when monitoring very fast processors such as digital signal processors. ***** SEE ORIGINAL DOCUMENT ***** Fig. 2 illustrates the technique of this disclosure wherein a 14- bit address bus of a digital signal processor (DSP) is monitored. This DSP has a separate instruction address bus and data address bus. The instructions are stored in a 27-bit wide instruction memory which is randomly accessible (RAM). Aside from the 27 bits, this RAM has an extra bit added. This bit is called the breakpoint bit. Wherever a

breakpoint is desired, the breakpoint bit at that particular memory address, is set. The extra bit in RAM is not extra overhead due to standard RAM sizes. In fact, this takes advantage of previously unused RAM bits. - As the DSP runs, it fetches instructions from instruction RAM. As **instructions** are fetched, the **breakpoint bit** is tested. If the breakpoint bit is found to be set, an 'address compare' function has been realized without the extra logic and time delay inherent to conventional address compare circuits. - Another feature of this design is the ability to have not one, but several breakpoints, without adding any additional logic. Multiple breakpoints is a valuable feature that would require several additional registers if it were implemented in a conventional address compare circuit.

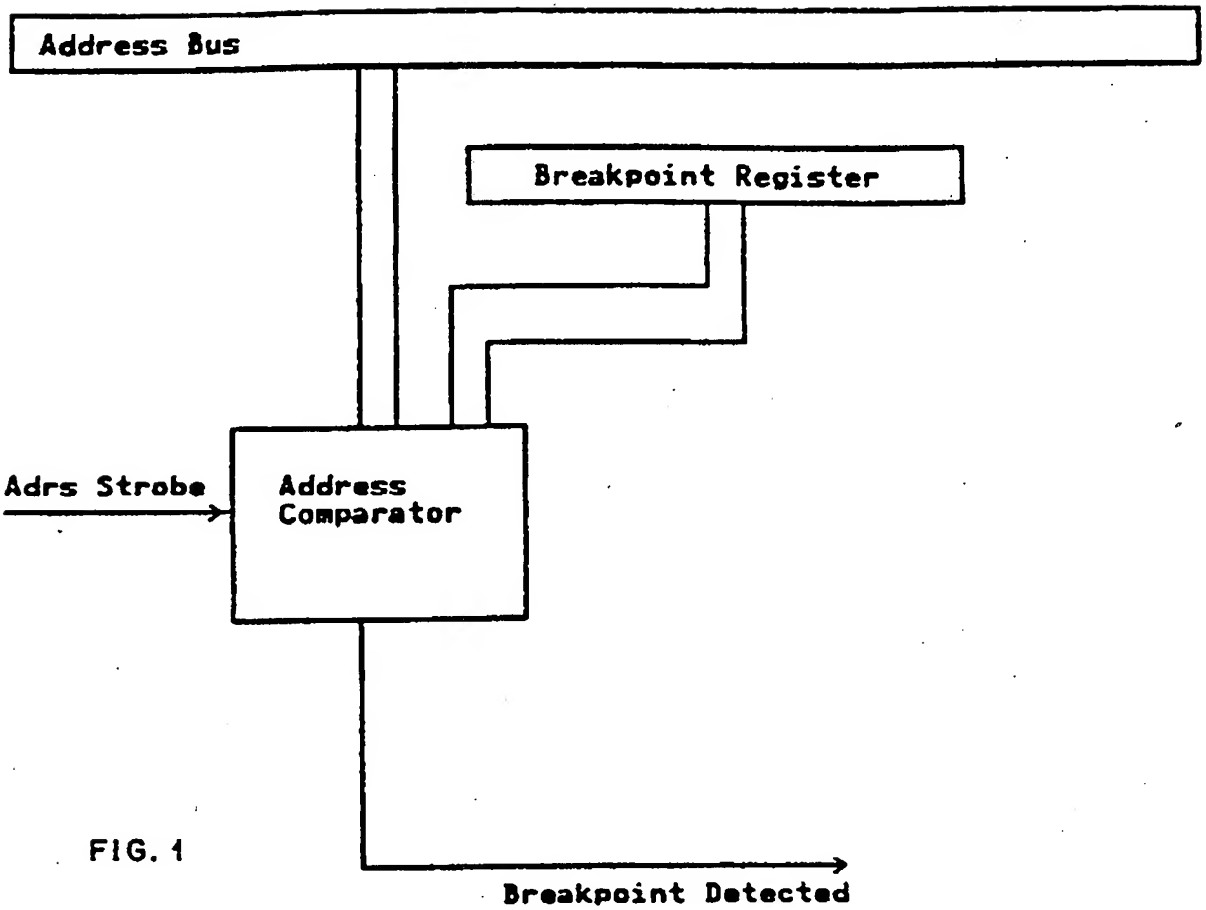
Address Bus
Breakpoint Register
Adrs Strobe
Address Comparator
Breakpoint Detected

FIG. 1

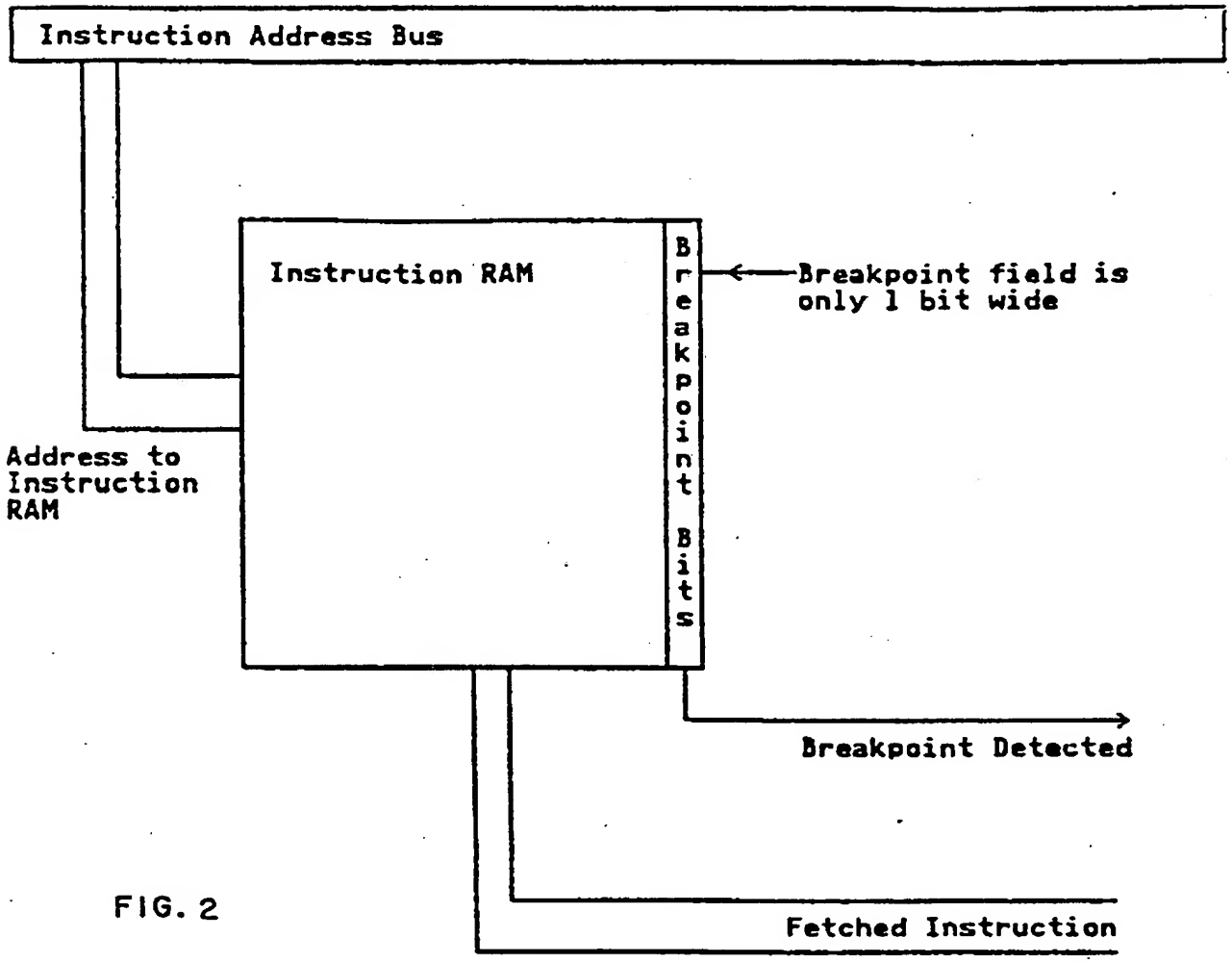
Instruction Address Bus
Instruction RAM
Breakpoint Bits
Breakpoint field is only 1 bit wide
Address to Instruction RAM
Breakpoint Detected
Fetched Instruction

FIG. 2

ADVANCED 80386 PROGRAMMING TECHNIQUES

James L. Turley

Osborne McGraw-Hill
Berkeley, California

Osborne McGraw-Hill
2600 Tenth Street
Berkeley, California 94710
U.S.A.

For information on translations and book distributors outside of the U.S.A., please write to Osborne McGraw-Hill at the above address.

A complete list of trademarks appears on page 499.

Advanced 80386 Programming Techniques

234567890 DODO 898

ISBN 0-07-881342-5